

Model 653

Very Low Jitter LVPECL or LVDS Clock

Features

- Ceramic Surface Mount Package
- Very Low Phase Jitter Performance, 500fs Maximum
- Fundamental or 3rd Overtone Crystal Design
- Frequency Range 10 – 320MHz *
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-418



Part Dimensions:
5.0 × 3.2 × 1.2mm • 62.00mg

Applications

- SerDes
- Storage Area Networking
- Broadband Access
- SONET/SDH/DWDM
- PON
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

Standard Frequencies

- 25.00MHz
- 50.00MHz
- 100.00MHz
- 125.00MHz
- 155.52MHz
- 156.25MHz
- 161.1328MHz
- 187.50MHz
- 200.00MHz
- 212.50MHz
- 250.00MHz
- 312.50MHz

* Check with factory for availability.

Description

CTS Model 653 is a low cost, high performance clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M653 has excellent stability and very low jitter/phase noise performance.

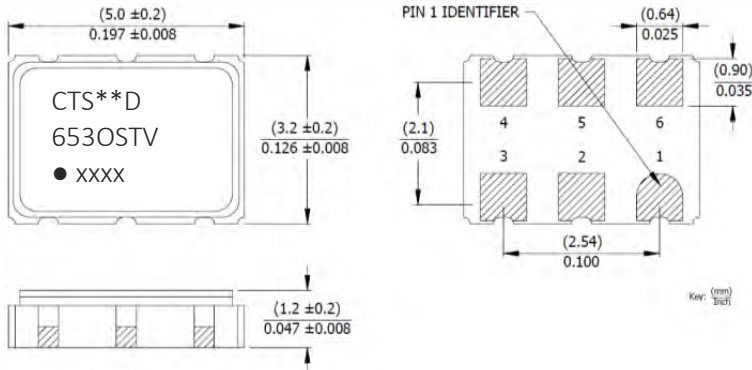
Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging																										
653	P	XXX or XXXX	3	I	3	T																										
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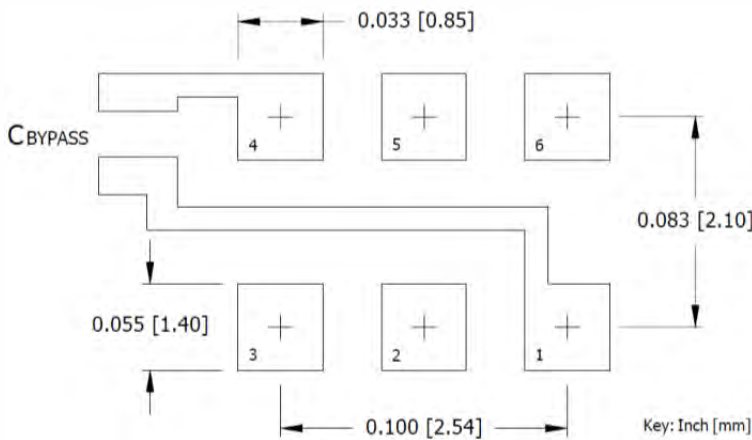
Notes:

- 1] Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2] Consult factory for availability of 6I Stability/Temperature combination.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.



1. ** - Manufacturing Site Code.
2. D - Date Code. See Table I for codes.
3. O - Output Type; P or E = LVPECL, L or V = LVDS.
ST - Frequency Stability/Temperature Code.
[Refer to Ordering Information]
4. V - Voltage Code; 3 = 3.3V, 2 = 2.5V.
5. xxxx - Frequency Code.
3-digits, frequencies below 100MHz
4-digits, frequencies 100MHz or greater
[See document 016-1454-0, Frequency Code Tables.]



1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. MSL = 1.

1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V _{CC}	Supply Voltage

Table I - Date Code

YEAR		MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
		2001	2005	2009	2013	2017												
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M		
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z		
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m		
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z		

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