SiT2018

High Temp, Single-Chip, One-Output Clock Generator

The Smart Timing Choice™

Features

- Frequencies between 1 MHz and 110 MHz accurate to 6 decimal places
- Operating temperature from -40°C to 125°C. For -55°C option, refer to SiT2020 and SiT2021
- Supply voltage of 1.8V or 2.5V to 3.3V
- Excellent total frequency stability as low as ±20 ppm
- Low power consumption of 3.6 mA typical at 1.8V
- LVCMOS/LVTTL compatible output
- 5-pin SOT23-5 package: 2.9mm x 2.8mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free
- **For AEC-Q100 clock generators, refer to SiT2024 and SiT2025**

Applications

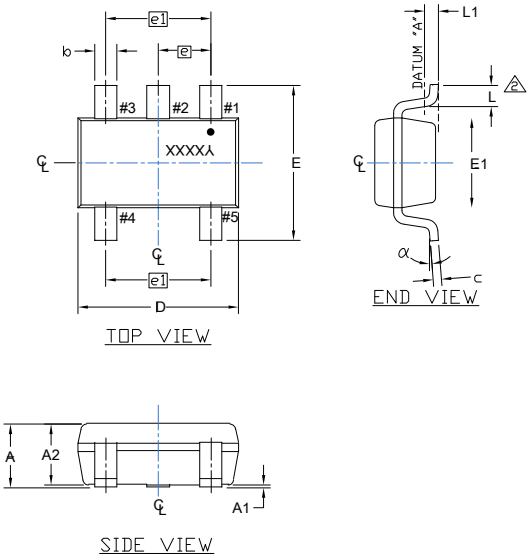
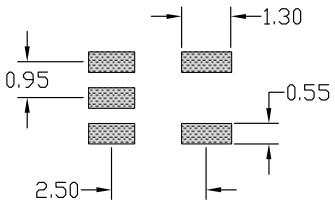
- Industrial, medical, automotive, avionics and other high temperature applications
- Industrial sensors, PLC, motor servo, outdoor networking equipment, medical video cam, asset tracking systems, etc.

Electrical Specifications

Table 1. Electrical Characteristics[1, 2]

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1	–	110	MHz	Refer to Table 14 for the exact list of supported frequencies list of supported frequencies
Frequency Stability and Aging						
Frequency Stability	F_stab	-20	–	+20	ppm	Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load (15 pF ± 10%).
		-25	–	+25	ppm	
		-30	–	+30	ppm	
		-50	–	+50	ppm	
Operating Temperature Range						
Operating Temperature Range (ambient)	T_use	-40	–	+105	°C	Extended Industrial
		-40	–	+125	°C	Automotive
Supply Voltage and Current Consumption						
Supply Voltage	Vdd	1.62	1.8	1.98	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
		2.25	–	3.63	V	
Current Consumption	Idd	–	3.8	4.5	mA	No load condition, f = 20 MHz, Vdd = 2.8V, 3.0V or 3.3V
		–	3.6	4.2	mA	No load condition, f = 20 MHz, Vdd = 2.5V
		–	3.4	4	mA	No load condition, f = 20 MHz, Vdd = 1.8V
OE Disable Current	I_od	–	–	4.4	mA	Vdd = 2.5V to 3.3V, OE = Low, output in high Z state.
		–	–	4.1	mA	Vdd = 1.8V, OE = Low, output in high Z state.
Standby Current	I_std	–	2.6	8.5	µA	Vdd = 2.8V to 3.3V, $\overline{ST}$ = Low, Output is Weakly Pulled Down
		–	1.4	5.5	µA	Vdd = 2.5V, $\overline{ST}$ = Low, Output is Weakly Pulled Down
		–	0.6	3.5	µA	Vdd = 1.8V, $\overline{ST}$ = Low, Output is Weakly Pulled Down
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	All Vdds
Rise/Fall Time	Tr, Tf	–	1.0	2.0	ns	Vdd = 2.5V, 2.8V, 3.0V or 3.3V, 20% - 80%
		–	1.3	2.5	ns	Vdd =1.8V, 20% - 80%
		–	1.0	3	ns	Vdd = 2.25V - 3.63V, 20% - 80%
Output High Voltage	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.0V or 3.3V) IOH = -3 mA (Vdd = 2.8V or 2.5V) IOH = -2 mA (Vdd = 1.8V)
Output Low Voltage	VOL	–	–	10%	Vdd	IOL = 4 mA (Vdd = 3.0V or 3.3V) IOL = 3 mA (Vdd = 2.8V or 2.5V) IOL = 2 mA (Vdd = 1.8V)

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[12]	Recommended Land Pattern (Unit: mm)[13]
2.90 x 2.80 mm SOT23-5 	

Notes:

12.Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
13. A capacitor value of 0.1 µF between Vdd and GND is required

Table 13. Dimension Table

Symbol	Min.	Nom.	Max.
A	0.90	1.27	1.45
A1	0.00	0.07	0.15
A2	0.90	1.2	1.30
b	0.30	0.35	0.50
c	0.14	0.153	0.20
D		2.90	
E		2.80	
E1		1.60	
e		0.95	
e1		1.90	
L	0.30	0.38	0.55
L1		0.25	
a	0°	–	8°