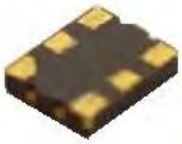

LV44J Series 3.3 V
LVDS Clock Oscillators

April 2017

Lead Free

- Pletronics' LV44J Series is a quartz crystal controlled precision square wave generator with LVDS output.
- Improved phase noise performance.
- Tape and Reel or cut tape packaging is available.
- 3.2 x 2.5 mm LCC Ceramic Package
- Enable/Disable Function on pad 1
- Disable function includes low standby power mode
- Fundamental and 3rd Overtone Crystals used
- Improved circuit to minimize oscillator issues such as multi-mode output signal.
- Lowest Jitter Product

*** BEST OPTION FOR LOW JITTER REQUIREMENTS**

Pletronics Inc. certifies this device is in accordance with the RoHS 6/6 (2011/65/EC) and WEEE (2002/96/EC) directives.

Pletronics Inc. guarantees the device does not contain the following:
Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
Weight of the Device: 0.09 grams
Moisture Sensitivity Level: 1 As defined in J-STD-020D.1
Second Level Interconnect code: e4

Absolute Maximum Ratings:

Parameter	Unit
V_{CC} Supply Voltage	-0.3V to +4.0V
Vi Input Voltage	-0.3V to V_{CC} + 0.3V
Vo Output Voltage	-0.3V to V_{CC} + 0.3V

Thermal Characteristics

The maximum die or junction temperature is 125°C
The thermal resistance junction to board is 30 to 50°C/Watt depending on the solder pads, ground plane and construction of the PCB.

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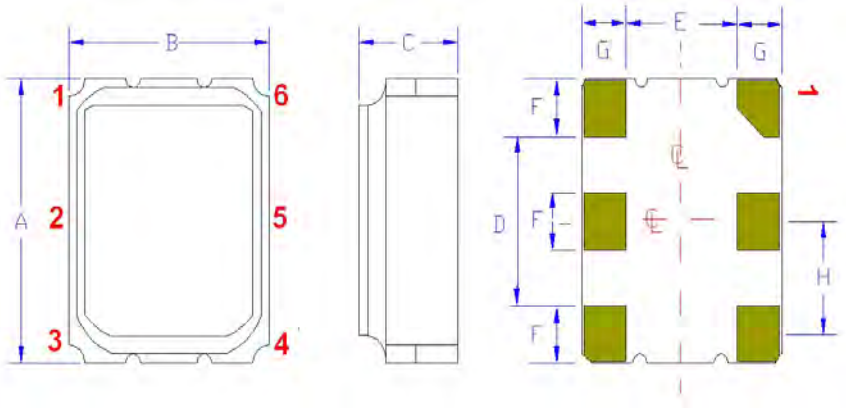
Mechanical:



	Inches	mm
A	0.125 ±0.004	3.20 ±0.10
B	0.098 ±0.004	2.50 ±0.10
C	0.040 max	1.00 max
D[1]	0.063	1.60
E[1]	0.051	1.30
F[1]	0.031	0.80
G[1]	0.024	0.60
H[1]	0.047	1.20

Contacts:
Gold 11.8 to 39.4 µinches (0.3 to 1.0µm) over
Nickel 50 to 350 µinches (1.27 to 8.89 µm)

[1] Typical dimensions

Not to Scale

Pad	Function	Note
1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. When this pad is < 'V disable', the output will be inhibited (high impedance state.) Recommend connecting this pad to V_{CC} if the oscillator is to be always on.
2	No connect	There is no internal connection to this pad
3	Ground (GND)	
4	Output	The outputs must be terminated, 100 ohms between the outputs is the ideal termination.
5	Output*	
6	Supply Voltage (V_{CC})	Recommend connecting appropriate power supply bypass capacitors as close as possible.

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Layout and application information

Recommend connecting Pad 1 and Pad 2 together to permit the design to accept Enable/Disable input on either pad

For Optimum Jitter Performance, Pletronics recommends:
- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.